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Oleksandr K. Teslenko¹, Candidate of Technical Sciences, Associate Professor of System Software and Specialized Computer Systems Faculty, E-mail: teslenko@scs.kpi.ua, ORCID: 0000-0002-5891-4345

Maksym Y. Bondarchuk¹, PhD student of System Software and Specialized Computer Systems Faculty, E-mail: bondarchuk.m.y@gmail.com, ORCID: 0000-0002-4861-6627

¹National Technical University of Ukraine “Igor Sikorsky Kyiv Polytechnic Institute”, 37 Peremohy Ave., Kyiv, Ukraine 03056

IMPLEMENTATION OF ARBITRARY BITNESS PERMUTATIONS IN ONE OF THE CLASSES OF LINEAR STRUCTURES

Abstract: Speed of transformation and simplicity of implementation are one of the key contributors in permutation researches. The paper reviews the implementation of arbitrary bitness permutation in the field of computer engineering on one of the classes of combination structures of linear complexity from the number of variables – one-dimensional cascades of structural units. The fact that the reflection formed by the specified linear structure is completely the same as the reflection of the corresponding Mealy finite state machine as a prototype of the structural module of the cascade is used. This allowed us to explore the properties of structural units and the cascade as a whole in the context of the concepts of the theory of digital automata. The implementation of arbitrary bitness permutations is based on usage of the connected graphs for state table and on usage of unique combinations without repeats for each row of output table. The purpose of this permutation is to convert large volumes of data in fast and simple way using hardware or software with the ability to be used in multiple areas of researches. The study of providing the bijectivity of the reflection and the equivalence analysis of permutations was performed. The algorithm of construction of finite-state machines for implementation of direct and inverted permutations is shown, as well as examples of state and output tables construction. Examples of hardware implementation using field-programmable gate arrays are given. The size of state and output tables for the software implementation is estimated. The number of unique bijective reflections and amount of key information for the investigated permutation in cryptographic transformations has been estimated. The theoretical speed of transformations of the bijective reflection is estimated for both field-programmable gate arrays and software implementation according to the modern indicators of types of computing devices memory speed. The practical verification of processing speed is made with software implementation. Areas of application of the investigated arbitrary bitness permutation are proposed.

Keywords: permutation functions; structural synthesis of finite state machines; Mealy machine; bijective reflection; field-programmable gate arrays

Introduction

Permutations (substitutes) are considered as functions of a single variable that provide a bijective reflection of input data at the output. Permutations are used when considering theoretical questions in different sections of mathematics (e.g. finite group theory, finite fields, combinatorics, etc.), and in practical development (for example in cryptographic transformation). Despite the considerable results of studies of permutations in mathematics [1], in computer engineering the implementation of substitutions has been studied to a lesser extent. In mathematics it is ordinary to characterize permutation by its degree – the number of elements of the input (output) set. In computer engineering, permutation can be characterized by the bitness b of the binary input data. In this case the degree of permutation is 2^b . The purpose of the work is creation and research of hardware and software means for implementation of permutations of arbitrary bitness. The problem is cost optimization and processing time while ensuring that the values of the result bits depend on all the input data bits, or at least on all previous input data bits. The usage of

such implementation of permutation gives the prospect of increasing efficiency in creating various data transformations in one or another criterion set.

Analysis of recent scientific publications and achievements

Hardware implementation methods of limited bitness permutations have been investigated in a number of papers [2-4] in particular [3] and [4] have the implementation results for any 8-bit permutations, as well as for 8-bit permutations class with special properties, both made on field-programmable gate arrays (FPGA). The software implementation of permutations of a limited bitness is simple and is used in cryptographic transformations [5-6]. The considered papers investigate the “permutation-implementation” approach: one or another class of permutations is formed and then the implementation of permutations of this class is determined. [7] proposes “implementation-permutation” approach to the implementation of permutations, which could be

described as follows: determines the linear complexity combinational structure from the bit of the input data, one-dimensional cascade of structural units (OCSU), and defines the classification of such structures: the classes of the simplest, simple, complex, unidirectional, bidirectional and regular.

Obviously, it is theoretically possible to implement permutations of arbitrary bitness with OCSU. This raises the following tasks: what should be the structural unit (SU) and how many and what permutations can be implemented on the OCSU of the appropriate class? In general, these problems are not solved.

The [8] shows that with the simplest unidirectional regular OCSU, 48 different substitutions of arbitrary bitness (with 2^b degree) ($b > 1$) can be implemented by changing the SU. 850 simple substitutions with 2^b degree ($b > 1$) can be implemented on the simplest bidirectional regular OCSU, as presented in [9]. The significant increase in the number of different permutations with a slight complication of OCSU allows predicting the effect-tiveness of further complications.

Problem formulation

This paper discusses the implementation of

arbitrary bitness permutations in the class of unidirectional complex regular OCSUs. The structural unit of the cascade consists of two combination schemes: the first one implements the value of signals at the primary outputs, and the second one implements the value of the signals at the side outputs. The inputs of both combination circuits receive signals from the primary and side inputs of the SU (Fig. 1) Obviously, this class of OCSU implements the reflection of the input data, which is the same with the reflection of the input sequences of the corresponding Mealy finite-state machine (FSM or FSA – finite-state automata). This allows us to use the automata theory [10] to solve the following problems:

- 1) define combinational circuits for the signals' formation at the outputs of the SU and implementation of permutations of arbitrary bitness (bijective reflections) on the OCSU;
- 2) define conditions for different OCSUs to implement the same permutations;
- 3) determine the number of different permutations that can be implemented on the OCSU of the selected class;
- 4) define inverted SU, that would provide the implementation of inverted permutation for given direct SU.

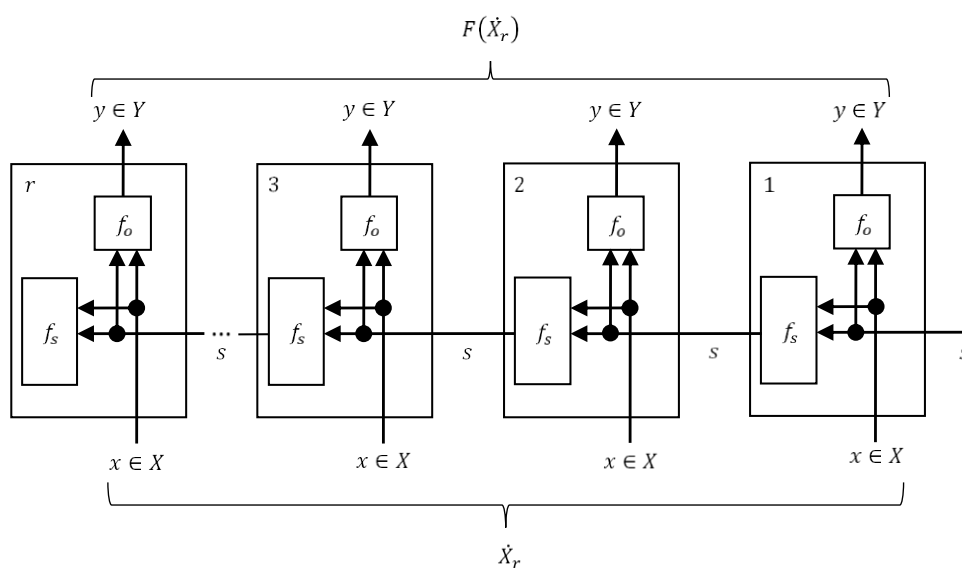


Fig. 1. Unidirectional OCSU for $F(\dot{X}_r)$ permutation implementation

Research Results

Terminology

Suppose we have a finite set of symbols called the input alphabet X of dimension n : $\{x_1, x_2, \dots, x_n\}$, a finite set of symbols called the output alphabet Y of dimension n : $\{y_1, y_2, \dots, y_n\}$, a finite set of states S of dimension m , a state transition function $f_s(x, s): S \times X \rightarrow S$, the output transition function $f_o(x, s): S \times X \rightarrow Y$ and the initial state $s_0 \in S$.

In the case when the machine is considered as a SU prototype, the input and output alphabets are the same, the values of n and m are degrees of two and the functions of outputs and states are implemented by the corresponding combination circuits. We will assume that state and output functions are fully defined. We will also assume that the machine is connected graph, which means, that it does not contain unreachable states and none of its states is equivalent to another [10]. In addition, an initial value is set at the side inputs of the first OCSU design module. This value corresponds to the initial state of the machine (Fig. 1).

Let us denote the set of all sequences of length r from the elements of the input alphabet by \dot{X}_r and by Y_r for the output one. The Mealy machine (respectively OCSU) maps the set \dot{X}_r to the set Y_r of OCSU ($\dot{X}_r \rightarrow \dot{Y}_r$).

Reflection bijectivity analysis

Machine implementation of the permutation (according to OCSU) means the implementation of a bijective reflection ($\dot{X}_r \rightarrow \dot{Y}_r$) at any value of r . In other words, different sequences of \dot{X}_r correspond to different sequences of \dot{Y}_r .

To eliminate the ambiguity of the permutation (bijective reflection) of arbitrary bitness, which is implementation by the FSA (or OCSU), we will hereafter denote it as $F(\dot{X}_r)$.

Two sequences of characters considered different if they differ at least in one character. If machine's reflection is not bijective for some r , it will not be bijective for any $r_1 > r$.

The loss state is called the state s_l for which exist $x_1, x_2 \in X$, where $x_1 \neq x_2$ and $f_o(s_l, x_1) = f_o(s_l, x_2)$. Taking this into account, the following theorems are given.

Theorem 1. The machine's reflection $f_A: \dot{X}_r \rightarrow \dot{Y}_r$ is bijective on \dot{X} if and only if the machine A does not contain loss states reached from the initial state s_0 in r steps [11-12].

Theorem 2. In order for OCSU to implement the $F(\dot{X}_r)$ permutation, it is required and sufficient that, for any signal at the side inputs of the SU, at the primary (not side) outputs, the combination circuit implements any substitution of the values of the signals at the primary inputs.

The bitness of the $F(\dot{X}_r)$ permutation is $b = r \log n$. The degree of permutation is n^r .

Equivalence analysis

Let $p(s)$ be some permutation of elements of the S set and let $p^{-1}(s)$ be the inverse permutation, that is, $p(p^{-1}(s)) = p^{-1}(p(s)) = s$.

Theorem 3. If for any machine A we create an automatic machine A_1 with the same alphabets X, Y, S and with the following functions $v_o(x, s) = f_o(x, p(s))$, $v_s(x, s) = p^{-1}(f_s(x, p(s)))$, and with the initial state $s_{0A} = p^{-1}(s_0)$, then machines A and A_1 will be equivalent.

Prove. Let x symbol be the input of A and A_1 . A_1 machine generates $v_o(x, s) = f_o(x, p(s))$ output symbol, and $v_s(x, s) = p^{-1}(f_s(x, p(s)))$ state. In the first iteration, the initial state of the machine A_1 is $s_{0A} = p^{-1}(s_0)$. So, we have

$$\begin{aligned} v_o(x, s) &= f_o(x, p(s)) = f_o(x, p(s_{0A})) \\ &= f_o(x, p^{-1}(s_0)) = f_o(x, s). \end{aligned}$$

A_1 will go into the state

$$p^{-1}\left(f_s\left(x, p(s_{0A})\right)\right) = p^{-1}\left(f_s\left(x, p(p^{-1}(s_0))\right)\right) = p^{-1}\left(f_s(x, s_0)\right).$$

The same happens for any number of the following input characters. Thus, both machines implement the same reflection, which means, they are equivalent [10].

Thus, in the OCSU class under consideration, there are $m!$ OCSUs that implement the same $F(\dot{X}_r)$ permutation, which is important when estimating the number of different permutations.

Structural unit construction algorithm

The basic algorithm for construction output tables is as follows. Output table rows are states. A random number generator is used to get a random character from the set of outputs. The generator produces the next output symbol. The character is added to the row of the table that does not contain this character. If the character produced by the generator exists in all rows, it is skipped. The algorithm ends when all rows are filled. The basic algorithm for forming the state table is as follows. A random number generator is used to get a random

$$\left(1 + \log \sum_{k=0}^{\infty} \frac{2^{\frac{m(m-1)}{2}}}{m!} k^m\right) \frac{m(n!)!}{(n! - m)!} \leq O(n, m) \leq \frac{m^{nm+1}(n!)!}{(n! - m)!}. \quad (1)$$

Note that the number of different permutations $F(\dot{X}_r)$ will be at least $m!$ times smaller, according to Theorem 2.

Software implementation processing speed estimations

To convert one character of the input sequence, three operations must be performed: two memory reads using indices from state and output tables and status change. The index is determined by the value of the current state and the input alphabet character as stated above. Status change is a memory write operation. Since no calculations are used, the direct and inverse transformations times are directly proportional to the speed of used memory (CPU cache levels L1, L2, L3, L4, random-access memory (RAM), read-only memory (ROM), external device, etc.).

Let's denote the speed of performing one operation with memory as v (MB/s).

Then the conversion time T of the input message with the length r of the input alphabet is calculated as

$$T = 4vr,$$

where: the factor 4 consists of one read operation from state table, one read operation from output

table, one read operation of the current state and one write operation of the new state.

Table 6 lists the memory capacity and maximum speed of different types of memory according to recent studies [16]. The amount of storage should be considered when evaluating the permutation appliance in accordance with Table 5.

Table 6. Speed and volume of memory types

| Memory type | Volume | Speed |
|-------------|-----------|----------|
| L1 cache | 128 KB | 700 Gbps |
| L2 cache | 1 MB | 200 Gbps |
| L3 cache | 6 MB | 100 Gbps |
| L4 cache | 128 MB | 40 Gbps |
| RAM | Gigabytes | 10 Gbps |
| ROM | Terabytes | 160 MB/s |

Table 7 shows the permutation processing time, depending on the type of memory, bitness of the input alphabet and the number of states. For cases when the maximum amount of memory at the time of article writing exceeds the requirements of Table 5, the time is marked by *.

Table 7. Theoretical time of permutation processing

| r | T L1, ns | T L2, ns | T L4, ns | T L5, ns | T RAM, ns | T ROM, ns |
|---------|------------|------------|------------|------------|-------------|-------------|
| 8 | 4,26E-02 | 1,49E-01 | 2,98E-01 | 7,45E-01 | 2,98E+00 | 4,66E+01 |
| 16 | 8,51E-02 | 2,98E-01 | 5,96E-01 | 1,49E+00 | 5,96E+00 | 9,31E+01 |
| 32 | 1,70E-01 | 5,96E-01 | 1,19E+00 | 2,98E+00 | 1,19E+01 | 1,86E+02 |
| 64 | 3,41E-01 | 1,19E+00 | 2,38E+00 | 5,96E+00 | 2,38E+01 | 3,73E+02 |
| 128 | 6,81E-01 | 2,38E+00 | 4,77E+00 | 1,19E+01 | 4,77E+01 | 7,45E+02 |
| 256 | 1,36E+00 | 4,77E+00 | 9,54E+00 | 2,38E+01 | 9,54E+01 | 1,49E+03 |
| 512 | 2,72E+00 | 9,54E+00 | 1,91E+01 | 4,77E+01 | 1,91E+02 | 2,98E+03 |
| 1024 | 5,45E+00 | 1,91E+01 | 3,81E+01 | 9,54E+01 | 3,81E+02 | 5,96E+03 |
| 2048 | 1,09E+01 | 3,81E+01 | 7,63E+01 | 1,91E+02 | 7,63E+02 | 1,19E+04 |
| 4096 | 2,18E+01 | 7,63E+01 | 1,53E+02 | 3,81E+02 | 1,53E+03 | 2,38E+04 |
| 8192 | 4,36E+01 | 1,53E+02 | 3,05E+02 | 7,63E+02 | 3,05E+03 | 4,77E+04 |
| 16384 | 8,72E+01 | 3,05E+02 | 6,10E+02 | 1,53E+03 | 6,10E+03 | 9,54E+04 |
| 32768 | 1,74E+02 | 6,10E+02 | 1,22E+03 | 3,05E+03 | 1,22E+04 | 1,91E+05 |
| 65536 | 3,49E+02 | 1,22E+03 | 2,44E+03 | 6,10E+03 | 2,44E+04 | 3,81E+05 |
| 131072 | 6,98E+02 | 2,44E+03 | 4,88E+03 | 1,22E+04 | 4,88E+04 | 7,63E+05 |
| 262144 | 1,40E+03 | 4,88E+03 | 9,77E+03 | 2,44E+04 | 9,77E+04 | 1,53E+06 |
| 524288 | 2,79E+03 | 9,77E+03 | 1,95E+04 | 4,88E+04 | 1,95E+05 | 3,05E+06 |
| 1048576 | 5,58E+03* | 1,95E+04 | 3,91E+04 | 9,77E+04 | 3,91E+05 | 6,10E+06 |
| 2097152 | 1,12E+04* | 3,91E+04 | 7,81E+04 | 1,95E+05 | 7,81E+05 | 1,22E+07 |
| 4194304 | 2,23E+04* | 7,81E+04 | 1,56E+05 | 3,91E+05 | 1,56E+06 | 2,44E+07 |
| 8388608 | 4,46E+04* | 1,56E+05 | 3,13E+05 | 7,81E+05 | 3,13E+06 | 4,88E+07 |

Appliance

The proposed implementations of permutations can be used in data compression [17], combination circuits optimization [8; 18], non-algorithmic implementation of encoders and decoders of fault-tolerant coding [19] and to increase efficiency of algorithms' software implementation [20]. The studied permutation has a wide range of applications and can theoretically be used in any device that requires, for example, high speed encryption and decryption.

Results comparison with existing counterparts

The effectiveness of the proposed solutions follows from the comparisons with known results.

In hardware implementations, for example, byte permutations in our case, it is enough to use $C = 8(d+w)/d$ LUTs, at the same time, the best implementations of the byte substitutions proposed in [4] require 19 LUTs. If we take $d = 4$, $w = 2$ ($n = 16$, $m = 4$), then we have $C = 12$ LUTs. If we want to implement two boolean functions with 5 variables and take $d = 2$, $w = 2$ ($n = 4$, $m = 4$), we will have $C = 8$ LUTs.

About time characteristics of software implementations. In [21], the implementation of high-bitness permutations using simple transformations in Galois fields is considered. The theoretical speed calculations are substantially inferior to those given in Table 7, since in our case we achieve speed of up to one million Mbps. There are no experimental results in [21].

Table 8 shows the results of the experiments (processing time T_r and processing speed ϑ_r) for the implementation of the bijective reflections for the $d = w = 8$ ($n = m = 256$) case, and the r value actually corresponds to the number of bytes of the file. The experiments were performed using DDR3 RAM and an Intel Core i7-6700K processor.

Experimental time of processing is lower than theoretical (especially when converting small amounts of data), because in modern multi-threaded operating systems it is difficult to gain monopoly access to system resources, especially cache when processing long-length files.

In [5] experimental data of time of cryptographic transformations by the "Kalyna" standard are given. The best results have a speed of about 2500 Mbps. Speeds in Table 8 in general exceed the results of "Kalyna". However, it should be noted that the conditions for conducting the experiment in [5] actually correspond to theoretical calculations. This is evidenced by usage of a cache that contained only one block (16 to 64 bytes) of the original message and encrypted only that block (in fact, electronic code book (ECB) mode). In our case, the theoretical speed is more than one million Mbps.

Table 8. Permutation's software implementation processing time and speed

| r | T_r , O3II, ns | ϑ_r , Mbps |
|---------|------------------|----------------------|
| 1024 | 3,06E+04 | 255,00 |
| 2048 | 3,46E+04 | 451,26 |
| 4096 | 4,26E+04 | 732,92 |
| 8192 | 5,14E+04 | 1216,55 |
| 16384 | 7,54E+04 | 1657,00 |
| 32768 | 1,18E+05 | 2110,82 |
| 65536 | 2,09E+05 | 2396,50 |
| 131072 | 3,94E+05 | 2541,13 |
| 262144 | 7,65E+05 | 2615,53 |
| 524288 | 1,50E+06 | 2672,66 |
| 1048576 | 3,06E+06 | 2612,61 |
| 2097152 | 5,78E+06 | 2769,95 |
| 4194304 | 1,17E+07 | 2743,38 |
| 8388608 | 2,12E+07 | 3023,83 |

Conclusions and prospects for further research

The obtained results allow conversion of files of any finite length. The number of different transformations increases faster than the exponent of the n and m parameters and does not depend on the file size. For example, at $n = m = 8$ (bitness of the SU data is only 3), the number of different $F(\hat{X}_r)$ permutations are estimated to be at least 10^{50} .

The studied implementation of the permutations provides good performance, although it does require memory space for the conversion table and the outputs. The results show that, in terms of the required amount of data, the output and state tables can be embedded even in the processor cache to provide high-speed conversion.

The subject of further research is the analysis of the strong cryptography of the proposed implementations of arbitrary bitness permutations and comparison of results with block cipher algorithms (it is clear that the studied function is faster, but has worse strong cryptography values, but it is not clear how much values will differ) and development of algorithms for different levels of cryptanalysis.

The prospect of further study may also be the consideration of a class of bidirectional OCSUs (Fig. 2 and Fig. 3), which are not considered in this paper because of too high memory requirements for large graph sizes.

Regarding providing bijection reflection in bidirectional SUs. For two states in both directions theoretically and practically the question is solved [9]. For more than two states, the solutions are not yet known.

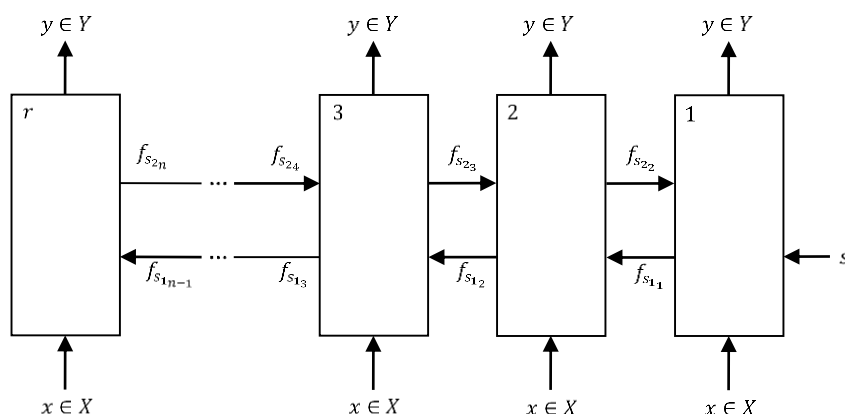


Fig. 2. Bidirectional OCSU for permutation

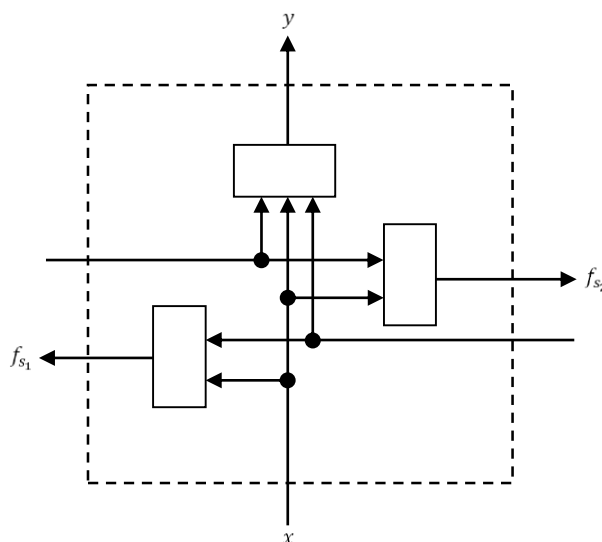


Fig. 3. One element of bidirectional OCSU for permutation

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¹**Тесленко, Олександр Кирилович**, кандидат техніч. наук, старший науковий співробітник, доцент кафедри системного програмування і спеціалізованих комп'ютерних систем,

E-mail: teslenko@scs.kpi.ua, ORCID: 0000-0002-5891-4345

¹**Бондарчук, Максим Юрійович**, аспірант кафедри системного програмування і спеціалізованих комп'ютерних систем, E-mail: bondarchuk.m.y@gmail.com, ORCID: 0000-0002-4861-6627

¹Національний технічний університет України «Київський політехнічний інститут імені Ігоря Сікорського», проспект Перемоги 37, Київ, Україна, 03056

РЕАЛІЗАЦІЯ ПІДСТАНОВОК ДОВІЛЬНОЇ РОЗРЯДНОСТІ В ОДНОМУ ІЗ КЛАСІВ ЛІНІЙНИХ СТРУКТУР

Анотація: Швидкість перетворення і простота реалізації є одними з ключових факторів підстановок. У статті розглянуто реалізацію підстановки довільної розрядності в області комп'ютерної інженерії на одному із класів комбінаційних структур лінійної складності від кількості змінних – одновимірних каскадів конструктивних модулів. Використано той факт, що відображення, яке формує вказана лінійна структура, повністю збігається з відображенням відповідного скінченного автомата Мілі як прототипу конструктивного модуля каскаду. Це дозволило досліджувати властивості конструктивних модулів та каскаду в цілому у розрізі понять теорії цифрових автоматів. Реалізація підстановок довільної розрядності полягає у використанні приведених автоматів для таблиці станів і використанні унікальних комбінацій без повторів для кожного рядку таблиці виходів. Метою реалізації даної підстановки є швидке перетворення даних великих об'ємів з можливістю застосування в кількох напрямках досліджень при простій реалізації на апаратному або програмному рівні. Виконано дослідження забезпечення бієктивності відображення та проведено аналіз еквівалентності відображень. Показано алгоритми формування автоматів для реалізації прямих та обернених підстановок, а також приклади формування таблиць переходів та виходів. Наведено приклади апаратної реалізації на програмованих логічних інтегральних схемах. Виконано оцінку кількості унікальних бієктивних відображень. Проведено теоретичну оцінку швидкості бієктивних відображень при реалізації на програмованих логічних інтегральних схемах, а також при програмній реалізації згідно з сучасними показниками швидкості видів пам'яті обчислювальних пристроїв для кожного виду. Наведено експериментальну оцінку, а також проведено практичну перевірку швидкості перетворення за допомогою програмної реалізації. Запропоновано області застосування досліджених реалізацій підстановок довільної розрядності.

Ключові слова: функції підстановок; автомат Мілі; бієктивне відображення, програмовані логічні інтегральні схеми

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¹**Тесленко, Александр Кириллович**, кандидат техніч. наук, старший научный сотрудник, доцент кафедры системного программирования и специализированных компьютерных систем,

E-mail: teslenko@scs.kpi.ua, ORCID: 0000-0002-5891-4345

¹**Бондарчук, Максим Юрьевич**, аспирант кафедры системного программирования и специализированных компьютерных систем, E-mail: bondarchuk.m.y@gmail.com, ORCID: 0000-0002-4861-6627

¹Национальный технический университет Украины «Киевский политехнический институт имени Игоря Сикорского», проспект Победы 37, Киев, Украина, 03056

РЕАЛИЗАЦИЯ ПОДСТАНОВОК ПРОИЗВОЛЬНОЙ РАЗРЯДНОСТИ В ОДНОМ ИЗ КЛАССОВ ЛИНЕЙНЫХ СТРУКТУР

Аннотация: Скорость преобразования и простота реализации являются одними из ключевых факторов подстановок. В статье рассмотрены реализацию подстановки произвольной разрядности в области компьютерной инженерии на одном из классов комбинационных структур линейной сложности от количества переменных – одномерных каскадов конструктивных модулей. Использован тот факт, что отображение, которое формирует указанная линейная структура, полностью совпадает с отображением соответствующего конечного автомата Мили как прототипа конструктивного модуля каскада. Это позволило исследовать свойства конструктивных модулей и каскада в целом в разрезе понятий теории цифровых автоматов. Реализация подстановок произвольной разрядности заключается в использовании приведенных автоматов для таблицы состояний и использовании уникальных комбинаций без повторов для каждого строке таблицы выходов. Целью реализации данной подстановки является быстрое преобразование данных больших объемов с возможностью применения в нескольких направлениях исследований при простой реализации на аппаратном или программном уровне. Выполнены исследования обеспечения биективности отражения и проведен анализ эквивалентности отражений. Показано алгоритмы формирования автоматов для реализации прямых и обратных подстановок, а также примеры формирования таблиц переходов и выходов. Приведены примеры аппаратной реализации на программируемых логических интегральных схемах. Выполнена оценка объема таблиц переходов и выходов для аппаратной и программной реализации. Выполнена оценка количества уникальных биективных отражений. Проведено теоретическую оценку скорости биективных отражений при реализации на программируемых логических интегральных схемах, а также при программной реализации согласно современным показателям скорости видов памяти вычислительных устройств для каждого вида. Приведены экспериментальную оценку, а также проведено практическую проверку скорости преобразования с помощью программной реализации. Предложено области применения исследованных реализаций подстановок произвольной разрядности.

Ключевые слова: функции подстановок; автомат Мили; биективное отображения, программируемые логические интегральные схемы.



Oleksandr Teslenko, Candidate of Technical Sciences

Research field: system programming, cryptography,
design of specialized computer systems



Maksym Bondarchuk, PhD student

Research field: cryptography, automata theory,
heuristics, artificial intelligence